NB3V110xC Series

3.3V/2.5V/1.8V LVCMOS Low Skew Fanout Buffer Family

ON Semiconductor®

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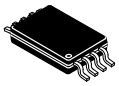


TSSOP−8
DT SUFFIX
CASE 948S

TSSOP−14
DT SUFFIX
CASE 948G

TSSOP−16
DT SUFFIX
CASE 948F

WDFN8, 2x2
MT SUFFIX
CASE 511AT

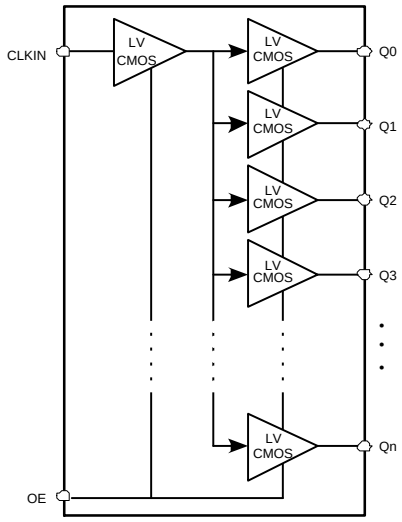
Description

The NB3V110xC are a modular, high−performance, low−skew, general purpose LVCMOS clock buffer family. The family of devices is designed with a modular approach. Four different fan−out variations, 1:2, 1:3, 1:4, 1:6 and 1:8, are available. All of the devices are pin compatible to each other for easy handling. All family members share the same high performing characteristics like low additive jitter, low skew, and wide operating temperature range. The NB3V110xC supports an asynchronous output enable control (OE) which switches the outputs into a low state when OE is low. The NB3V110xC devices operate in a 3.3 V, 2.5 V and 1.8 V environment and are characterized for operation from −40°C to 105°C.

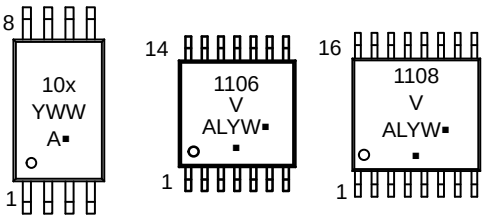
Features

- Operating Temperature Range: –40°C to 105°C
- High−Performance 1:2, 1:3, 1:4, 1:6, 1:8 LVCMOS Clock Buffer
- Available in 8−, 14−, 16−Pin TSSOP and WDFN8 Packages
- Very Low Output−to−Output Skew < 50 ps
- Very Low Additive Jitter < 200 fs
- Supply Voltage: 3.3 V, 2.5 V or 1.8 V
- f_{max} = 250 MHz for 3.3 V; f_{max} = 180 MHz for 2.5 V; f_{max} = 133 MHz for 1.8 V
- These Devices are Pb−Free and are RoHS Compliant

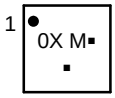
BLOCK DIAGRAM



MARKING DIAGRAMS



TSSOP−8 **TSSOP−14** **TSSOP−16**



WDFN8

A	= Assembly Location
M	= Date Code
L	= Wafer Lot
Y	= Year
W, WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 9 of this data sheet.

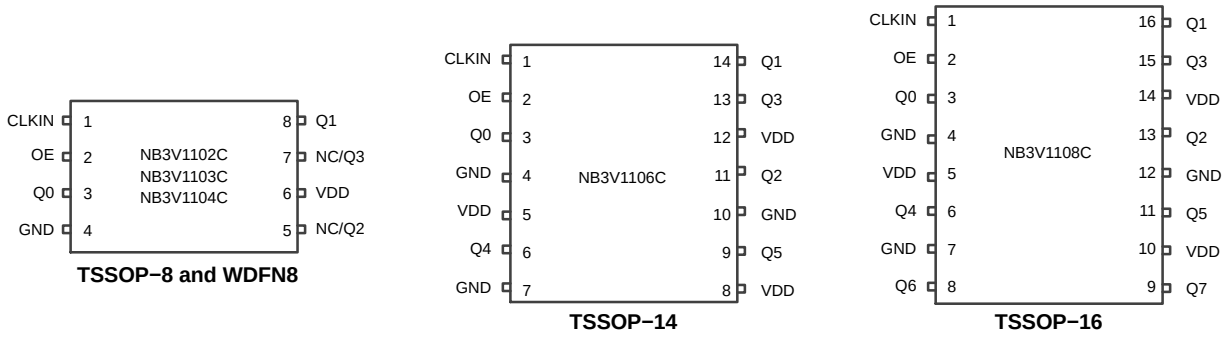


Figure 1. Pin Configuration

Table 1. PIN DESCRIPTION

Devices	LVCMOS Clock Input	LVCMOS Clock Output Enable	LVCMOS Clock Output	Device Supply Voltage	Device Ground
	CLKIN	OE	Q0, Q1, ... Q7	V_{DD}	GND
NB3V1102C	1	2	3, 8	6	4
NB3V1103C	1	2	3, 8, 5	6	4
NB3V1104C	1	2	3, 8, 5, 7	6	4
NB3V1106C	1	2	3, 14, 11, 13, 6, 9	5, 8, 12	4, 7, 10
NB3V1108C	1	2	3, 16, 13, 15, 6, 11, 8, 9	5, 10, 14	4, 7, 12

NOTE: Pins not mentioned in the table are NC.

Table 2. OUTPUT LOGIC TABLE

INPUTS		OUTPUTS
CLKIN	OE	Qn
X	L	L
L	H	L
H	H	H

Table 3. ATTRIBUTES

Characteristic		Value	Unit
ESD Protection	Human Body Model (HBM) per ANSI/ESDA/JEDEC JS−001−2014 Charged Device Model (CDM) per ANSI/ESDA/JEDEC JS−002−2014	5000 1500	V V
Moisture Sensitivity, Indefinite Time Out of Dry Pack (Note 1)		Level 1	−
Meets or exceeds JEDEC Spec JESD78D (LU) IC Latchup Test			

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with a large copper heat spreader (20 mm^2, 2 oz.)

Table 4. ABSOLUTE MAXIMUM RATINGS (Note 2)
Over operating free−air temperature range (unless otherwise noted)

Symbol	Condition		Value	Unit
V_{DD}	Supply Voltage Range		–0.5 to 4.6	V
V_{IN}	Input Voltage Range (Note 3)		–0.5 to V_{DD} + 0.5	V
V_O	Output Voltage Range (Note 3)		–0.5 to V_{DD} + 0.5	V
I_{IN}	Input Current		±20	mA
I_O	Continuous Output Current		±50	mA
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	TSSOP−8	151.2*	°C/W
		TSSOP−14	104*	
		TSSOP−16	32*	
			110**	
		WDFN8	190**	
θ_{JC}	Thermal Resistance (Junction−to−Case top)	TSSOP−8	35	°C/W
		TSSOP−14	8.6	
		TSSOP−16	10	
		WDFN8	10	
T_J	Maximum Junction Temperature		125	°C
T_{STG}	Storage Temperature Range		–65 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with a large copper heat spreader (20 mm^2, 2 oz.)
3. For additional information, see Application Note AND8003/D.
*JEDEC51.7 four layer PCB with 100 sqmm, 2 oz with two 80x80x1oz ground planes.
**JEDEC51.3 two layer PCB with 100 sqmm, 2 oz.

Table 5. RECOMMENDED OPERATING CONDITIONS
Over operating free−air temperature range (unless otherwise noted)

Symbol	Condition		Min	Typ	Max	Unit
V_{DD}	Supply voltage range	3.3 V supply	3.0	3.3	3.6	V
		2.5 V supply	2.3	2.5	2.7	
		1.8 V supply	1.71	1.8	1.89	
V_{IL}	Low−level input voltage	V_{DD} = 3.0 V to 3.6 V			$V_{DD}/2 – 600$	mV
		V_{DD} = 2.3 V to 2.7 V			$V_{DD}/2 – 400$	
		V_{DD} = 1.71 V to 1.89 V			$0.3xV_{DD}$	V
V_{IH}	High−level input voltage	V_{DD} = 3.0 V to 3.6 V	$V_{DD}/2 + 600$			mV
		V_{DD} = 2.3 V to 2.7 V	$V_{DD}/2 + 400$			
		V_{DD} = 1.71 V to 1.89 V	$0.7xV_{DD}$			V
V_{th}	Input threshold voltage	V_{DD} = 2.3 V to 3.6 V	$V_{DD}/2$			V
		V_{DD} = 1.71 V to 1.89 V	$V_{DD}/2$			V
t_r / t_f	Input slew rate (Note 4)		1		4	V/ns
t_w	Minimum pulse width at CLKIN	V_{DD} = 3.0 V to 3.6 V	1.8			ns
		V_{DD} = 2.3 V to 2.7 V	2.75			
		V_{DD} = 1.71 V to 1.89 V	3.75			
f_{CLK}	LVCMOS clock Input Frequency	V_{DD} = 3.0 V to 3.6 V	DC		250	MHz
		V_{DD} = 2.3 V to 2.7 V	DC		180	
		V_{DD} = 1.71 V to 1.89 V	DC		133	
T_A	Operating free−air temperature		–40		105	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
4. Guaranteed by Design.

Table 6. DEVICE CHARACTERISTICS Over recommended operating free−air temperature range (unless otherwise noted) (Note 5)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
OVERALL PARAMETERS FOR ALL VERSIONS						
I_{DD}	Static device current	OE = V_{DD}; CLKIN = 0 V or V_{DD}; I_O = 0 mA; V_{DD} = 3.6 V			0.2	mA
		OE = V_{DD}; CLKIN = 0 V or V_{DD}; I_O = 0 mA; V_{DD} = 2.7 V			0.2	
		OE = V_{DD}; CLKIN = 0 V or V_{DD}; I_O = 0 mA; V_{DD} = 1.89 V			0.2	
I_{PD}	Power down current	OE = 0 V; CLKIN = 0 V or V_{DD}; I_O = 0 mA; V_{DD} = 3.6 V, 2.7 V or 1.89 V (For 1102C, 1103C, 1104C)			60	μA
		OE = 0 V; CLKIN = 0 V or V_{DD}; I_O = 0 mA; V_{DD} = 3.6 V, 2.7 V or 1.89 V (For 1106C, 1108C)			75	
C_{PD}	Power dissipation capacitance per output (Note 6)	V_{DD} = 3.3 V; f = 10 MHz		9		pF
		V_{DD} = 2.5 V; f = 10 MHz		9		
		V_{DD} = 1.8 V; f = 10 MHz		9		
I_I	Input leakage current at OE	V_I = 0 V or V_{DD}, V_{DD} = 3.6 V or 2.7 V			± 8	μA
	Input leakage current at CLKIN				± 8	
	Input leakage current at OE, CLKIN	V_I = 0 V or V_{DD}, V_{DD} = 1.89 V			± 8	
R_{OUT}	Output impedance	V_{DD} = 3.3 V		40		Ω
		V_{DD} = 2.5 V		45		
		V_{DD} = 1.8 V		60		
f_{OUT}	Output frequency	V_{DD} = 3.0 V to 3.6 V	DC		250	MHz
		V_{DD} = 2.3 V to 2.7 V	DC		180	
		V_{DD} = 1.71 V to 1.89 V	DC		133	
OUTPUT PARAMETERS FOR V_{DD} = 3.3 V ± 0.3 V						
V_{OH}	High−level output voltage	V_{DD} = 3 V, I_{OH} = –0.1 mA	2.9			V
		V_{DD} = 3 V, I_{OH} = –8 mA	2.5			
		V_{DD} = 3 V, I_{OH} = –12 mA	2.2			
V_{OL}	Low−level output voltage	V_{DD} = 3 V, I_{OL} = 0.1 mA			0.1	V
		V_{DD} = 3 V, I_{OL} = 8 mA			0.5	
		V_{DD} = 3 V, I_{OL} = 12 mA			0.8	
t_{PLH}, t_{PHL}	Propagation delay (Note 7)	CLKIN to Qn	0.8		2.0	ns
$t_{sk(o)}$	Output skew (Note 7)	Equal load of each output 85°C			50	ps
		Equal load of each output 105°C			60	
t_r/t_f	Rise and fall time	20%–80% (V_{OH} − V_{OL})	0.12		0.8	ns
t_{DIS}	Output disable time (Note 7)	OE to Qn			6	ns
t_{EN}	Output enable time (Note 7)	OE to Qn			6	ns
$t_{sk(p)}$	Pulse skew; $t_{PLH(Qn)} – t_{PHL(Qn)}$ (Note 8)	To be measured with input duty cycle of 50%			180	ps
$t_{sk(pp)}$	Part−to−part skew	Under equal operating conditions for two parts			0.5	ns
$T_{jit(\phi)}$	Additive jitter rms	12 kHz...20 MHz f_{OUT} = 100 MHz			100	fs
		12 kHz...20 MHz f_{OUT} = 156.25 MHz				

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. All typical values are at respective nominal V_{DD}. For switching characteristics, outputs are terminated to 50 Ω to V_{DD}/2 (see Figure 2).
6. This is the formula for the power dissipation calculation.
   Ptot = Pstat + Pdyn + PCload [W] $P_{stat} = V_{DD} \times I_{DD}$ [W]
   $P_{dyn} = C_{PD} \times V_{DD}2 \times f \times n$ [W]
   $P_{Cload} = C_{load} \times V_{DD}2 \times f \times n$ [W]
   n = Number of switching output pins
7. With rail to rail input clock.
8. $t_{sk(p)}$ depends on output rise− and fall−time (t_r/t_f). The output duty−cycle can be calculated: odc = $(t_{w(OUT)} \pm t_{sk(p)})/t_{period}$; $t_{w(OUT)}$ is pulse−width of ideal output waveform and tperiod is $1/f_{OUT}$.

Table 7. DEVICE CHARACTERISTICS (continued)
Over recommended operating free−air temperature range (unless otherwise noted) (Note 5)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
OUTPUT PARAMETERS FOR V_{DD} = 2.5 V ± 0.2 V						
V_{OH}	High−level output voltage	V_{DD} = 2.3 V, I_{OH} = –0.1 mA	2.2			V
		V_{DD} = 2.3 V, I_{OH} = –8 mA	1.7			
V_{OL}	Low−level output voltage	V_{DD} = 2.3 V, I_{OL} = 0.1 mA			0.1	V
		V_{DD} = 2.3 V, I_{OL} = 8 mA			0.5	
t_{PLH}, t_{PHL}	Propagation delay (Note 10)	CLKIN to Qn		1.8		ns
$t_{sk(o)}$	Output skew (Note 10)	Equal load of each output 85°C			50	ps
		Equal load of each output 105°C			60	
t_r/t_f	Rise and fall time	20%–80% (V_{OH} − V_{OL})	0.12		1.2	ns
t_{DIS}	Output disable time (Note 10)	OE to Qn			10	ns
t_{EN}	Output enable time (Note 10)	OE to Qn			10	ns
$t_{sk(p)}$	Pulse skew ; $t_{PLH(Qn)} – t_{PHL(Qn)}$ (Note 9)	To be measured with input duty cycle of 50%			220	ps
$t_{sk(pp)}$	Part−to−part skew	Under equal operating conditions for two parts			1.2	ns
$tjit_{(\phi)}$	Additive jitter rms	12 kHz...20 MHz f_{OUT} = 100 MHz			150	fs
		12 kHz...20 MHz f_{OUT} = 156.25 MHz			100	
OUTPUT PARAMETERS FOR V_{DD} = 1.8 V ± 5%						
V_{OH}	High−level output voltage	V_{DD} = 1.71 V, I_{OH} = –0.1 mA	1.6			V
		V_{DD} = 1.71 V, I_{OH} = –4 mA	0.75xV_{DD}			
V_{OL}	Low−level output voltage	V_{DD} = 1.71 V, I_{OL} = 0.1 mA			0.1	V
		V_{DD} = 1.71 V, I_{OL} = 4 mA			0.25xV_{DD}	
t_{PLH}, t_{PHL}	Propagation delay (Note 10)	CLKIN to Qn	1.8		3.5	ns
$t_{sk(o)}$	Output skew (Note 10)	Equal load of each output			75	ps
t_r/t_f	Rise and fall time	20%–80% (V_{OH} − V_{OL})	0.17		1.2	ns
t_{DIS}	Output disable time (Note 10)	OE to Qn			10	ns
t_{EN}	Output enable time (Note 10)	OE to Qn			10	ns
$t_{sk(p)}$	Pulse skew ; $t_{PLH(Qn)} – t_{PHL(Qn)}$ (Note 9)	To be measured with input duty cycle of 50%			450	ps
$t_{sk(pp)}$	Part−to−part skew	Under equal operating conditions for two parts			1.2	ns
$tjit_{(\phi)}$	Additive jitter rms	12 kHz...20 MHz, f_{OUT} = 100 MHz			200	fs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

9. $t_{sk(p)}$ depends on output rise− and fall−time (t_r/t_f). The output duty−cycle can be calculated: odc = ($t_{w(OUT)} \pm t_{sk(p)}$)/t_{period}; $t_{w(OUT)}$ is pulse−width of ideal output waveform and tperiod is 1/f_{OUT}.
10. With rail to rail input clock.

PARAMETERS MEASUREMENT INFORMATION

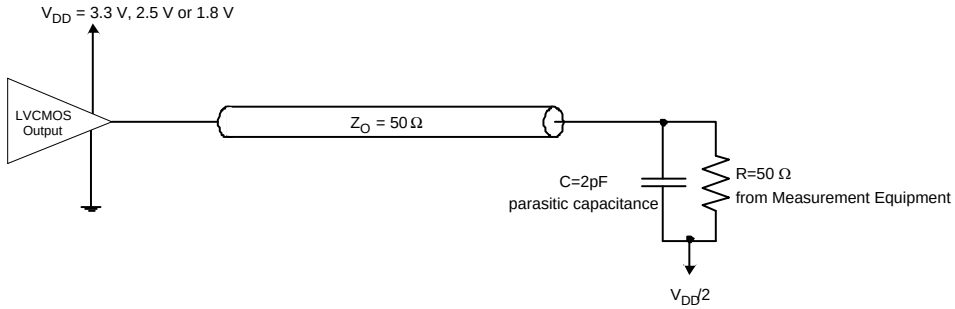


Figure 2. Test Load Circuit

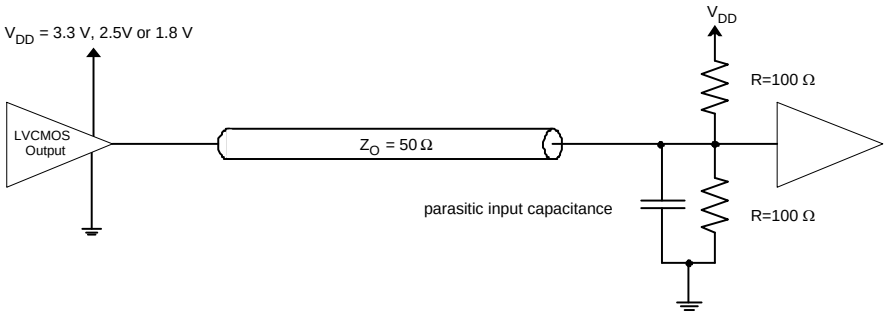


Figure 3. Application Load with 50 Ω Line Termination

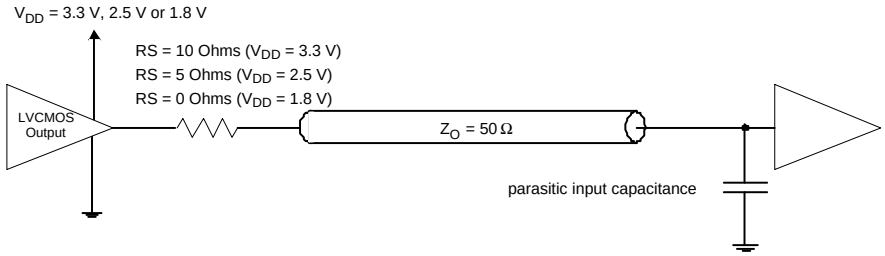


Figure 4. Application Load with Series Line Termination

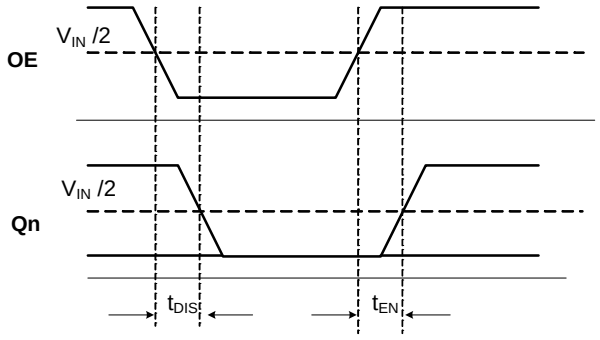


Figure 5. t_{DIS} and t_{EN} for Disable Low

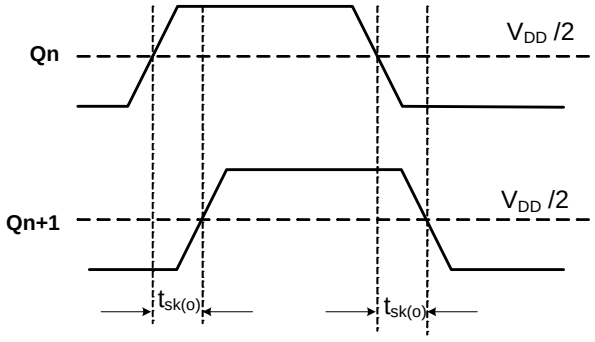


Figure 6. Output Skew $t_{Sk(o)}$

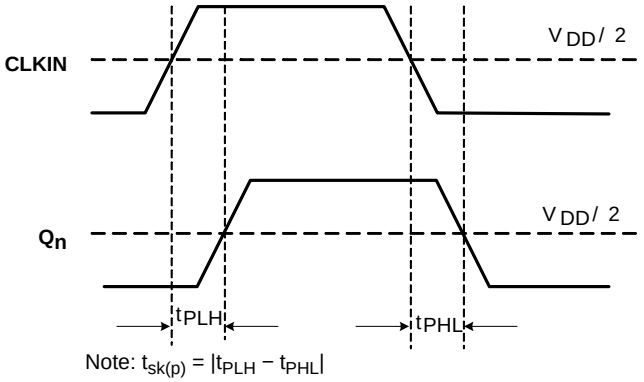


Figure 7. Pulse Skew $t_{sk(p)}$ and Propagation Delay t_{PLH}/t_{PHL}

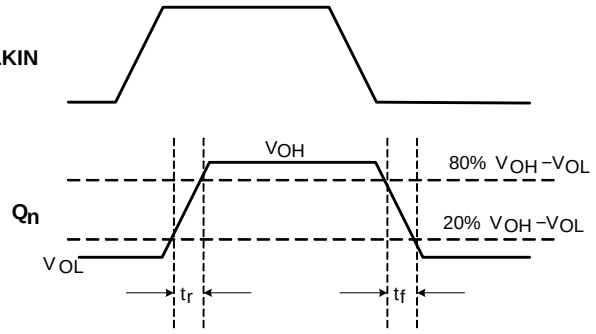


Figure 8. Rise/Fall Times t_r /t_f

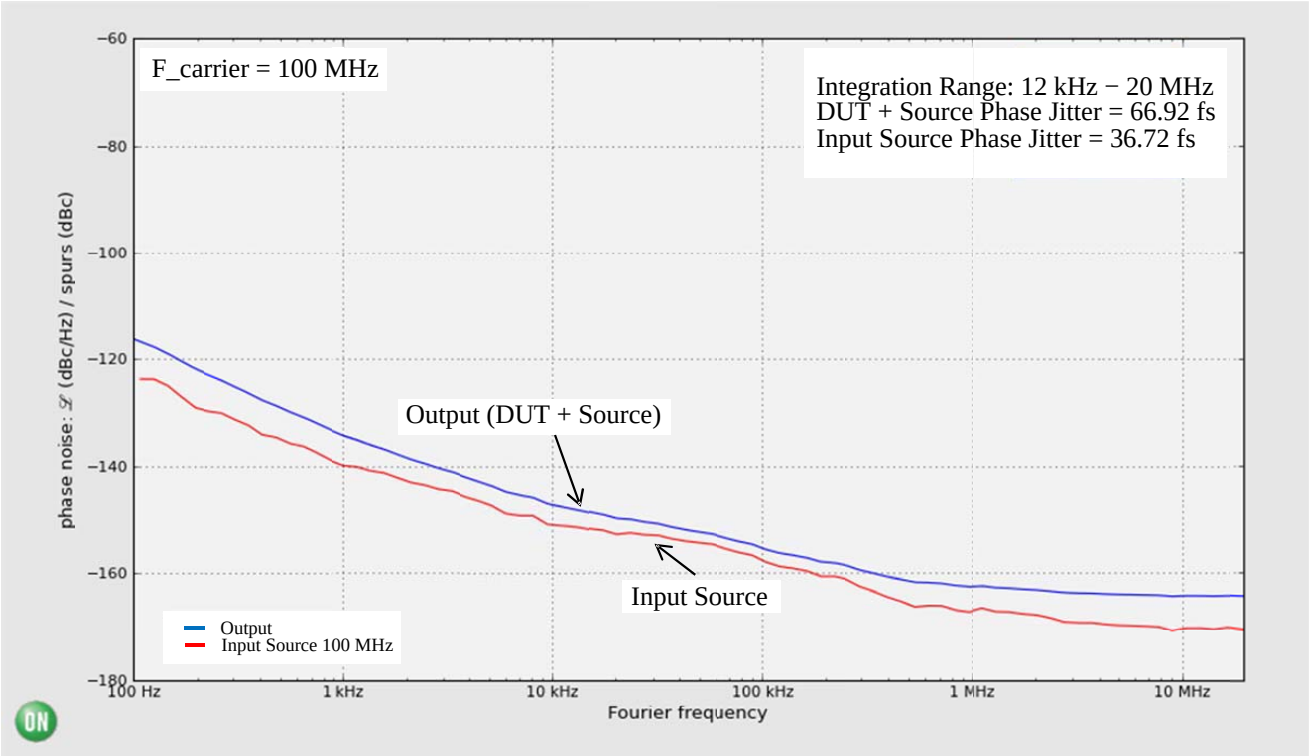


Figure 9. Typical NB3V110xC Phase Noise Plot at $f_{Carrier}$ = 100 MHz, V_{DD} = 3.3 V, 25°C

The above phase noise data was captured using Agilent E5052A/B. The data displays the input phase noise and output phase noise used to calculate the additive phase jitter at a specified integration range. The additive RMS phase jitter contributed by the device (integrated between 12 kHz and 20 MHz) is 55.94 fs. The additive RMS phase jitter performance of the fan out buffer is highly dependent on the phase noise of the input source.

To obtain the most precise additive phase noise measurement, it is vital that the source phase noise be notably lower than that of the DUT. If the phase noise of the source is greater than the noise floor of the device under test, the source noise will dominate the additive phase jitter calculation and lead to an incorrect negative result for the additive phase noise within the integration range. The Figure above is a good example of the NB3V110xC source generator phase noise having a significantly lower floor than the DUT and results in an additive phase jitter of 55.94 fs.

$$\text{Additive RMS phase jitter} = \sqrt{\text{RMS phase jitter of output}^2 - \text{RMS phase jitter of input}^2}$$

$$55.94\ \text{fs} = \sqrt{66.92\ \text{fs}^2 - 36.72\ \text{fs}^2}$$

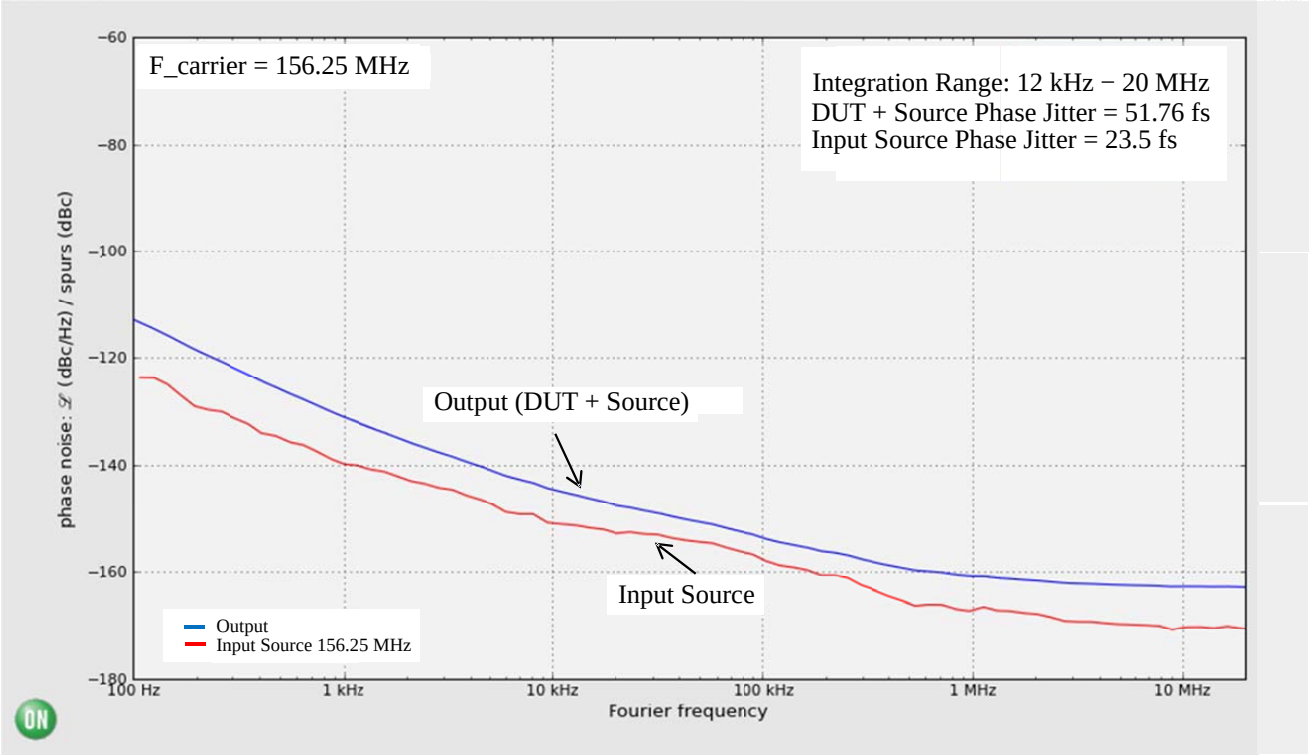


Figure 10. Typical NB3V110xC Phase Noise Plot at $f_{Carrier}$ = 156.25 MHz, V_{CC} = 3.3 V V, 25°C

The additive RMS phase jitter contributed by the device (integrated between 12 kHz and 20 MHz) is 46.11 fs.

$$\text{Additive RMS phase jitter} = \sqrt{\text{RMS phase jitter of output}^2 - \text{RMS phase jitter of input}^2}$$

$$46.11\ \text{fs} = \sqrt{51.76\ \text{fs}^2 - 23.5\ \text{fs}^2}$$

Figures 9 and 10 were created with measured data from Agilent−E5052A/B Signal Source Analyzer using ON Semiconductor Phase Noise Explorer web tool. This free application enables an interactive environment for advanced phase noise and jitter analysis of timing devices and clock tree designs. To see the performance of NB3V110xC beyond conditions outlined in this datasheet, please visit the ON Semiconductor Green Point Design Tools homepage.

Table 8. ORDERING INFORMATION

Device	Marking	Package	Shipping†
NB3V1102CDTR2G	102	TSSOP−8 (Pb−Free)	2500 / Tape & Reel
NB3V1103CDTR2G	103		
NB3V1104CDTR2G	104		
NB3V1102CMTTBG	02	WDFN8 (Pb−Free)	3000 / Tape & Reel
NB3V1104CMTTBG	04		
NB3V1106CDTR2G	1106 V	TSSOP−14 (Pb−Free)	2500 / Tape & Reel
NB3V1108CDTR2G	1108 V	TSSOP−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NOTE: Please contact your ON Semiconductor sales representative for availability of parts in tube.

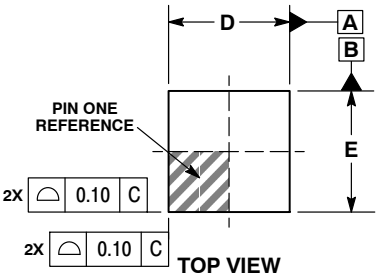
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

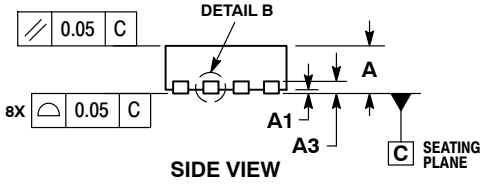
SCALE 4:1

WDFN8 2x2, 0.5P
CASE 511AT−01
ISSUE O

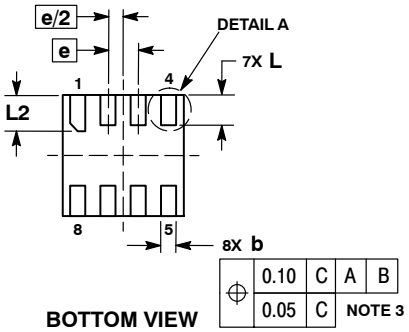
DATE 26 FEB 2010



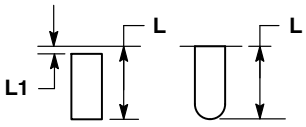
TOP VIEW



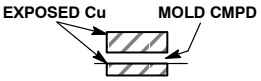
SIDE VIEW



BOTTOM VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

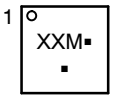


DETAIL B
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
E	2.00 BSC	
e	0.50 BSC	
L	0.40	0.60
L1	---	0.15
L2	0.50	0.70

GENERIC MARKING DIAGRAM*

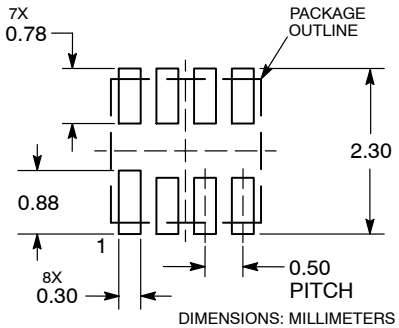


XX = Specific Device Code
M = Date Code
▪ = Pb−Free Device

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



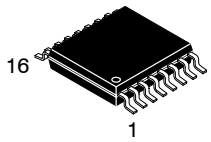
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON48654E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**WDFN8, 2X2, 0.5 P**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

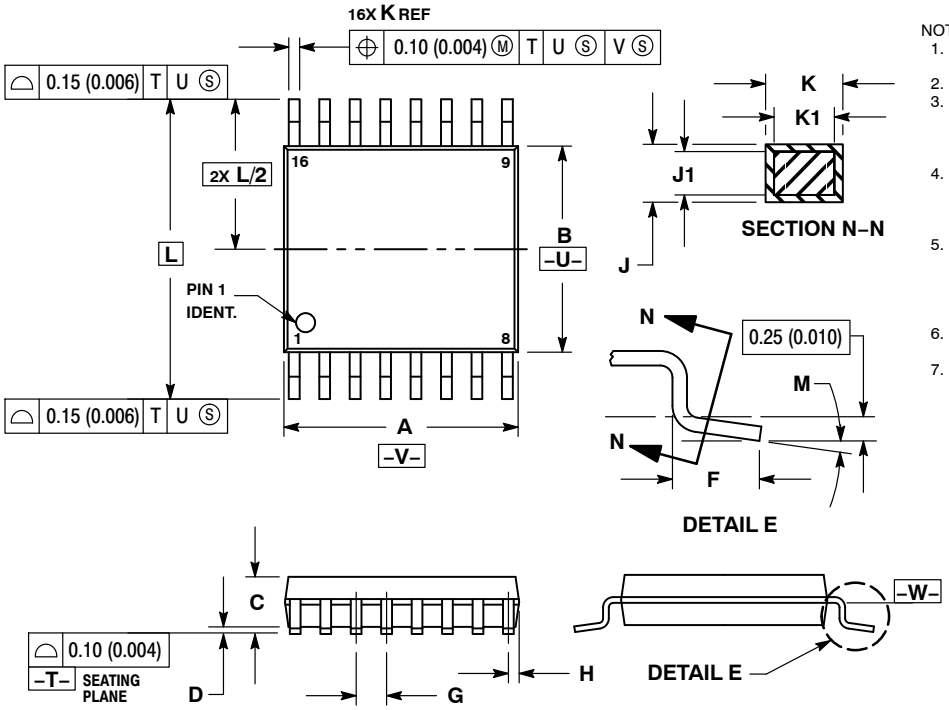
ON Semiconductor®



SCALE 2:1

TSSOP−16
CASE 948F−01
ISSUE B

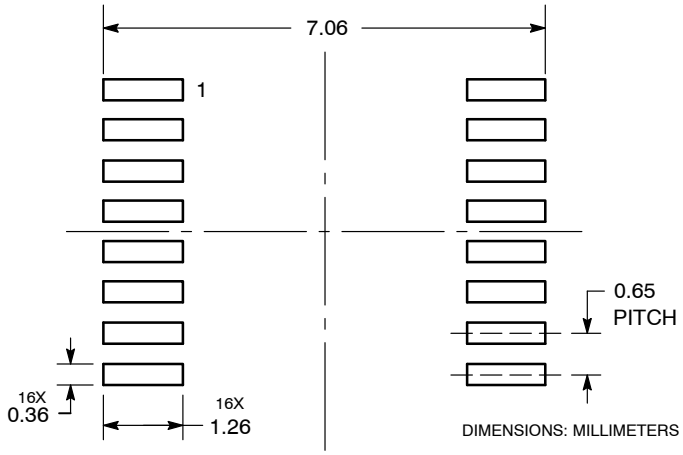
DATE 19 OCT 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

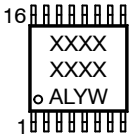
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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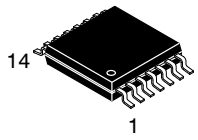
DESCRIPTION:	TSSOP−16	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

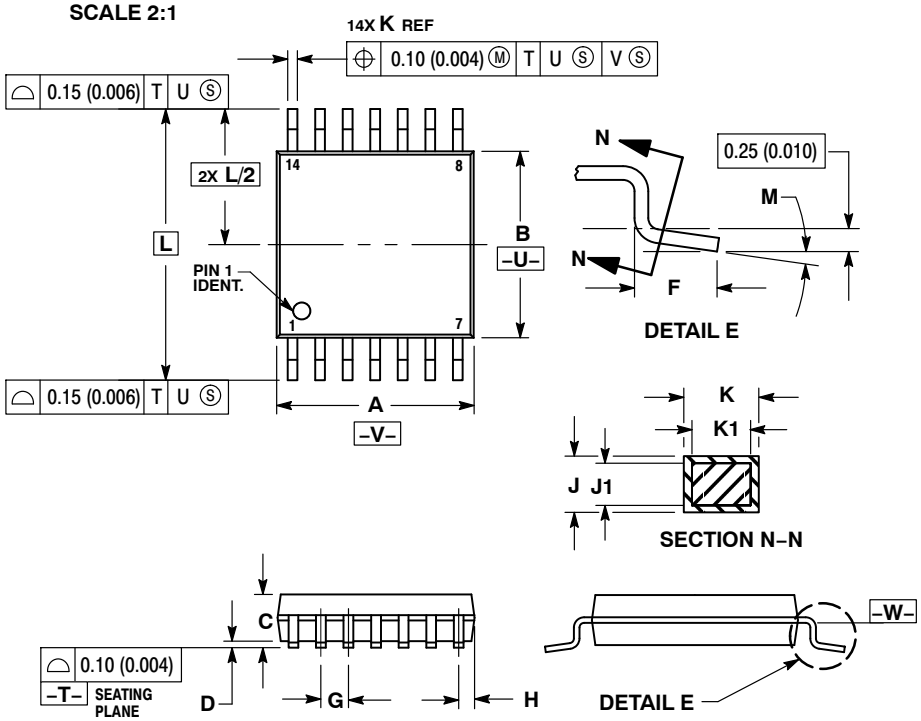
ON Semiconductor®

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016



SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
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7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
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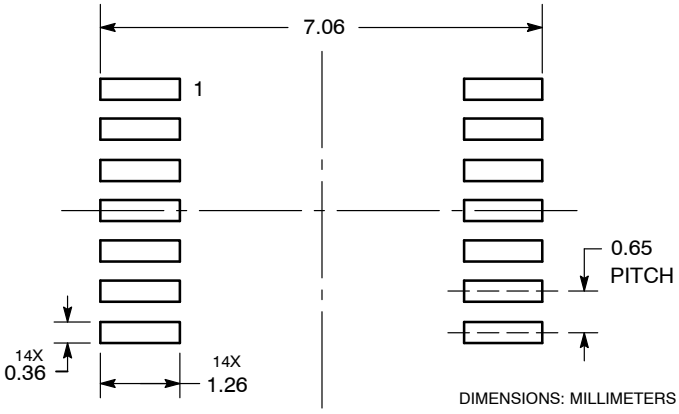
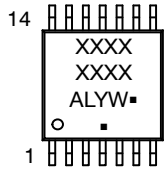
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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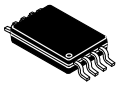
DESCRIPTION:	**TSSOP−14 WB**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TSSOP−8
CASE 948S−01
ISSUE C

DATE 20 JUN 2008



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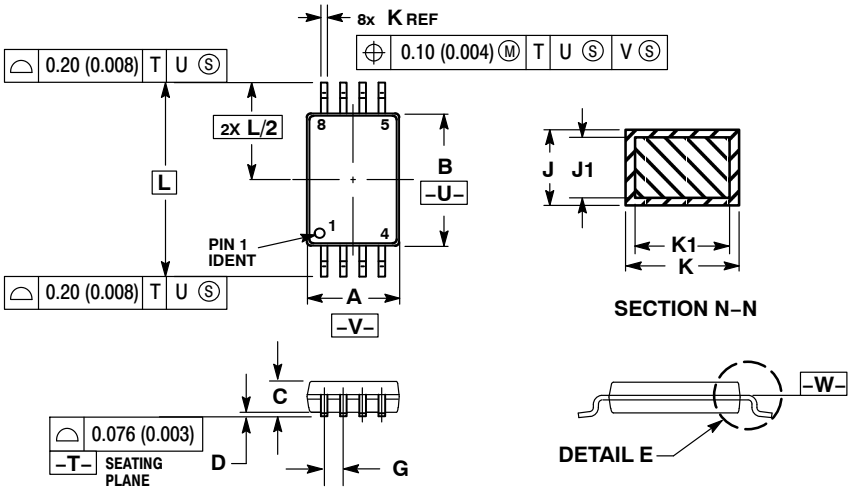

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
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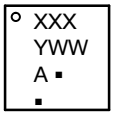
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65 BSC		0.026 BSC	
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	TSSOP−8	PAGE 1 OF 2

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION.	18 APR 2000
A	ADDED MARKING DIAGRAM INFORMATION. REQ. BY V. BASS.	13 JAN 2006
B	CORRECTED MARKING DIAGRAM PIN 1 LOCATION AND MARKING. REQ. BY C. REBELLO.	13 MAR 2006
C	REMOVED EXPOSED PAD VIEW AND DIMENSIONS P AND P1. CORRECTED MARKING INFORMATION. REQ. BY C. REBELLO.	20 JUN 2008

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